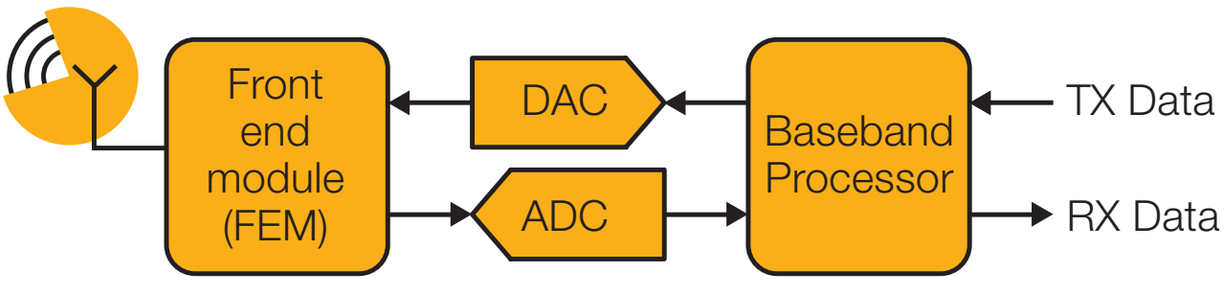
INTERLLIGENT
RF & Microwave Solutions

Training seminar programme

RF ADCs and DACs

2-day (18 study hours) seminar

Includes in-depth theoretical background, animated presentation, and classroom exercises



RF Training

Test Equipment

RF Components & Systems

Engineering Services

RF Ventures Incubator

RF is our Business... Signal us!

Introduction

Broadband analogue to digital converters (ADCs) and digital to analogue converters (DACs) are key building blocks in modern transceiver design. This seminar discusses some of their unique attributes and their influence on RF system design. In particular, it covers their unique frequency transfer function and its RF system implications, SNR limitations due to quantization and jitter, and frequency planning considerations - all in respect of real-IF and zero-IF transceivers that include ADCs and DACs.

Short form syllabus with time allocations

Subject / Covered content	Time allocated (hours)
1 / Broadband ADC fundamentals	2
2 / Baseband and IF Sampling	2
3 / Broadband DAC fundamentals	2
4 / Signal to quantization noise ratio (SQNR)	2
5 / Signal to aperture jitter voltage noise ratio (SJNR)	2
6 / Dynamic performance metrics for broadband converters	1
7 / Non transparent ADCs and DACs	1
8 / Overview of {ADC/ DAC + RF front end} system engineering considerations	2
9 / ADC / DAC measurements set-ups	1
10 / Analogue ports interfacing	1
11 / Classroom summary exercise	2
Total study duration	**18 hours**

Target audience

The target audience for this seminar consists of RF & microwave system engineers, wireless hardware experts and electronics engineers who deal with the design and testing of wireless transceivers.

Presenter

The seminar will be presented by **Mr. Oren Hagai**, the founder of INTERLLIGENT RF and Microwave Solutions. Bio available online at: https://www.linkedin.com/in/4x1vi

Detailed syllabus with suggested time allocations

Subject 1 | Broadband ADC fundamentals | 2 Hours

Classification and properties of ADC types

- 'Transparent ADCs' (code output describes present sample's value only).
- 'Non-Transparent ADCs' (code output refers also to prior samples).

Common ADC architectures

Transparent ADC implementation technologies

- Flash implementation, Digital ramp implementation, Successive approximation (SAR) implementation, Pipelined ADC implementation, Time interleaved ADC architectures

Non-transparent ADC implementation technologies

- Sigma-delta ADCs

The sampler block

- Sample and hold (S&H) vs. track and hold (T&H) mechanisms
- Mathematical equivalent model for a 'sample and hold' (S&H) sampler.
- Time domain illustration of the ideal sampling process.
- Frequency domain properties of the ideal sampling process: The frequency transfer function of a S&H sampler (Nyquist zones plot)

The quantizer block

- Linear (uniform) vs. nonlinear quantizers
- Implementation of a linear FLASH quantizer
- The input voltage to output code transfer function
- The connection between spectral purity to quantizer linearity and transfer function

Subject 2 | Baseband and IF Sampling | 2 hours

Baseband sampling

- The power spectral density (PSD) of a real-valued 'generalized baseband signal'
- The Nyquist-Shannon baseband sampling rule (with graphical interpretation)
- Receiver architectures that require baseband sampling
- Anti-aliasing filtering considerations for a baseband sampling ADC
- Over-sampling of baseband signals: system trade-offs.

IF sampling (subsampling)

- The Nyquist-Shannon baseband sampling rule
- Receiver architectures that require baseband sampling
- How and why to oversample and subsample at the same time

Frequency planning considerations in real-IF receivers with an ADC

- Frequency, bandwidth and sampling rate limitations which apply on IF signals
- Identifying and filtering 'dangerous' input frequencies (which fold into the desired signal's digital spectrum).
- Determining the required order of the anti-aliasing filter by the receiver's ACPR
- Selection of the Nyquist zone of operation: Jitter versus flicker noise trade-offs

Subject 3 | Broadband DAC fundamentals | 2 hours

Introduction to broadband DACs

- Clarifying the huge difference between the theoretical frequency responses of ADCs and DACs: DAC's Sinc lowpass response vs. ADC's flat frequency response
- Why DACs can be seen as 'precision devices', unlike most ADCs?

Common transparent DAC architectures

- The R-2R ladder (binary-weighted) DAC
- The current steering DAC

DAC's output spectra, frequency response and reconstruction filtering

- Obtaining the frequency response of an ideal DAC from its sampling rate
- Dynamic range reduction and spectral distortions for the DAC's output signal
- Baseband (mathematical) equalization techniques vs. analogue equalization filters
- Reconstruction filter considerations

Pushing up the bandwidth – "RF DACs"

- Return to zero, Non return to zero and dual return to zero pulse waveforms (filters)
- Selecting the optimal waveform (filter) per Nyquist zone

Subject 4 | Signal to quantization noise ratio (SQNR) | 2 hours

Maximum achievable SQNR for a transparent ADC

Quantization error and quantization noise

- The voltage quantization error and its relation with the quantizer's transfer function
- Conditions for treating deterministic quantization errors as additive random noise
- Autocorrelation, PSD and first order statistics of the quantization noise
- FFT refresher and the concept of 'baseband normalized power' for sampled signals
- Overall quantization noise power within the 'FFT visible range' (first Nyquist zone)
- Improving the quantization noise floor by oversampling (SQNR enhancements)
- Practical trade-offs in oversampling broadband ADCs: SQNR vs. power consumption

Acquired signal's power

- ADC transducer gain, formulating the baseband normalized power of a given analogue input waveform in terms of the ADC's parameters
- The motivation for full-scale acquisition for maximizing the output SQNR
- The concepts of 'power-reference waveforms' and 'waveform power ratio' (WPR)

Maximum achievable SQNR

- Formulating the maximum achievable SQNR for transparent ADC, for a given waveform, a given oversampling ratio and a given back-off from the ADC's full-scale
- Practical recommendations for back-offs taken from the ADC's full scale, with respect to the radio channel's model, modulation type, PAPR and CCDF.

Subject 5 | Signal to aperture jitter voltage noise ratio (SJNR) | 2 hours

Phase noise and jitter

- Definitions and metrics of phase noise and jitter, random vs. deterministic jitter
  Phase noise to Jitter conversion: Obtaining the sampling clock's RMS jitter from its phase noise L(Δf) plot, using Perceval's theorem
- Practical recommendations for phase noise integration bandwidth boundaries (relevant phase noise integration offsets from carrier) for practical jitter calculations
- Phase noise and jitter as multiplicative processes (signal power invariant effects)

Aperture jitter voltage noise

- Definition and graphical time-domain interpretation of aperture jitter voltage noise
- Why 'jitter hurts more' at higher analogue input frequencies
- How not to confuse the additive aperture jitter voltage noise with the multiplicative phase noise and jitter processes

Signal to aperture jitter voltage noise (SJNR) for a CW tone

- Calculating the overall power of the aperture jitter voltage noise, for a CW input
- Formulating the SJNR for a given RMS clock jitter and input analogue frequency

Subject 6 | Dynamic performance metrics for broadband converters | 1 hour

Converter's overall dynamic performance metrics

- Dynamic performance metrics vs. static performance metrics of a converter
- Dynamic metrics overview: $SQNR_{max}$, SJNR, SNR_{max}, SFDR, ENOB, SINAD, THD

Maximum achievable output SNR

- Calculation of the maximum achievable SNR at the converter's output (SNR_{max})

Effective number of bits (ENOB)

- Definition of ENOB
- Formulation of ENOB in terms of the SNR_{max} and in terms of the converter's SFDR

ADC Noise figure

- ADC noise density terms expressed in explained and translated into dBm/Hz

Spectral purity

- How and why quantization creates spur signals, converter's spur chart, identifying the causes for spur signals and harmonics
- Definitions of SFDR, THD and SINAD
- Applying dithering for improving spectral purity

Practical converter's figure of merits

- Sampling rate vs. power
- ENOB vs. power
- The B. Murmann 'ADC performance survey'

Subject 7 | Non transparent ADCs and DACs | 1 hours

Introduction to non-transparent (Sigma-Delta) ADCs

- The 1 bit ADC concept and the Delta modulation (baseband line code): Delta, Adaptive-Delta and Predictive-Delta modulations
- Sigma delta modulation: modulator and demodulator block diagrams
- Deriving Sigma-Delta data converters from Sigma-Delta modulation.
- The Sigma-Delta ADC and DAC

Performance limitations and constrains in Sigma-Delta converters

- Granular (idle) quantization noise.
- Slope over-load distortions, and their frequency dependence.
- Signal and noise shaping: LPF signal transfer function vs. HPF noise transfer function.
- Effective number of bits calculation and measurements

Subject 8 | Overview of ADC/DAC+ RF front end system considerations | 2 hours

Overview of {ADC/ DAC + RF front end} engineering considerations

- Selection of ADCs and DACs suitable for a required system EVM and SNR.
- Selection of input Balun for the ADC converter's input, and setting the desired converter input impedance
- System linearity considerations and their relation to the ADC's input impedance and DAC's output impedance.
- Setting the overall gain of the receiving chain according to the converter full scale and the desired sensitivity.
- Considerations and trade-offs in the transceiver's frequency plan: Architecture selection (real-IF / zero IF / Weaver / Hartley), IF frequency, sampling rate and filtering.
- How does the anti-aliasing filter's response affect the receiver's noise figure?

Subject 9 | ADC / DAC measurements set-ups | 1 hours

ADC measurements and performance validation

- Test set-ups for the following measurements dynamic performance metrics: ADC Noise density, SINAD, SFDR, SNRmax, DNL, INL, Noise figure, IIP2, IIP3, NPR, Signal-to-aperture-jitter voltage noise ratio
- Measuring the Scc11 / Sdd11 of an ADC / DAC analogue port
- The influence of the FFT size and window function on the measurement result

Subject 10 | Analogue ports interfacing | 1 hours

Interfacing the ADC's / DAC's analogue ports

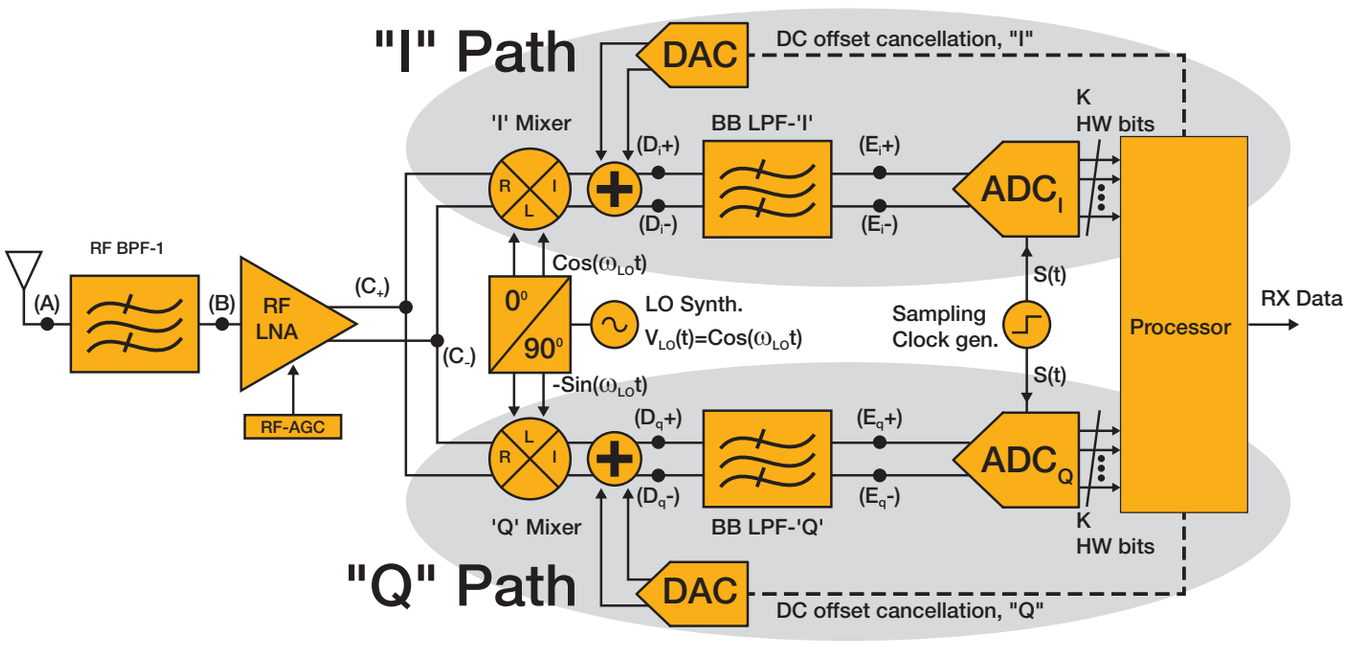
- Buffered vs. unbuffered ADCs / DACs
- Balanced vs. unbalanced inputs / outputs.
- Transformer matching: impedance matching vs. voltage gain, effects on linearity (IIP2, IIP3) and noise budget, common mode rejection ratio.
- Op-amp drivers: selecting the right topology considering impedance ratios, linearity.
- Op-amp vs. transformer interfacing trade-offs

Subject 11 | Classroom summary exercise | 2 hours

Classroom summary exercise

- Multiple choice questions
- Covering all the studied materials
- Involves real world RF system related trade-offs and considerations
- Design examples based on real life components and genuine datasheets

We hope to see you at the seminar!



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